Amendments to the Claims:

Listing of Claims:

1. (Currently Amended) A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of memory elements;

a plurality of field-effect programming transistors configured to program the memory elements with a programming current; and

a ~~bipolar device~~ plurality of bipolar devices, each of the bipolar devices associated with each of the memory elements and isolating the programming current in [[a]] each of the memory ~~element~~ elements from another memory element in the memory array.

2. (Currently Amended) The programmable memory of claim 1, wherein at least one of the memory ~~element~~ elements comprises a fuse element.

3. (Original) The programmable memory of claim 2, wherein the fuse element comprises at least one of tantalum aluminum, and tantalum aluminum nitride.

4. (Original) The programmable memory of claim 1, further comprising a plurality of layered heaters.

5. (Currently Amended) The programmable memory of claim 1, wherein at least one of the memory elements ~~element~~ comprises a floating gate element.

6. (Currently Amended) The programmable memory of claim 1, wherein each of the bipolar devices ~~device~~ comprises a pnp device.

7. (Original) The programmable memory of claim 6, further comprising a surrounding guard ring configured to isolate one pnp device from another pnp device.

8. (Original) The programmable memory of claim 7, wherein the surrounding guard ring comprises a p-type guard ring positioned around each pnp device.

9. (Original) The programmable memory of claim 7, wherein the surrounding guard ring comprises an n-type guard ring coupled to a high potential.

10. (Currently Amended) The programmable memory of claim 7, wherein each of the memory ~~element~~ elements is positioned within the surrounding guard ring.

11. (Currently Amended) The programmable memory of claim 7, wherein each of the memory ~~element~~ elements is positioned outside the surrounding guard ring.

12. (Currently Amended) The programmable memory of claim 6, wherein the memory array comprises rows and columns, wherein each of the pnp devices ~~device~~ has an n-type base, and wherein the pnp devices on each row are joined at the n-type base.

13. (Original) The programmable memory of claim 6, wherein the pnp devices are arranged in a plurality of rows and columns intersecting each other, and wherein the pnp devices on a row are isolated from the pnp devices of another row by a grounded p-type region.

14. (Original) The programmable memory of claim 6, wherein the pnp devices are arranged in a plurality of rows and columns intersecting each other, and wherein the pnp devices on a row are isolated from the pnp devices of another row by a high potential n-type region.

15. (Currently Amended) The programmable memory of claim 1, wherein each of the bipolar ~~device~~ devices comprises [[a]]an npn device.

16. (Currently Amended) The programmable memory of claim 1, wherein each of the bipolar ~~device~~ devices comprises a diode.

17. (Currently Amended) The programmable memory of claim 1, further comprising a memory density ~~comprising~~ based on a sum of areas occupied by the memory ~~element~~ elements and [[a]] the plurality of programming ~~transistor~~ transistors associated with the memory elements, wherein the memory density is at least 200 bits per square millimeter.

18. (Currently Amended) The programmable memory of claim 1, wherein the memory array has at least 128 memory elements, and each of the memory ~~element~~ elements has a resistance of at least 5 ohms on the inkjet printhead chip.

19. (Currently Amended) A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of ~~circuit~~ fuse elements arranged in rows and a plurality of ~~circuit~~ fuse elements arranged in columns intersecting the rows to thereby form a plurality of memory elements;

a plurality of field-effect programming transistors configured to program the memory elements with a programming current; and

a ~~biplolar element~~ plurality of bipolar elements, each of the bipolar elements coupled to each of the memory ~~element~~ elements and configured to isolate the programming current in each of the memory ~~element~~ elements from another memory element.

20. (Currently Amended) The programmable memory of claim 19, wherein each of the fuse ~~element~~ elements comprises at least one of tantalum aluminum, and tantalum aluminum nitride.

21. (Original) The programmable memory of claim 19, further comprising a plurality of layered heaters.

22. (Currently Amended) The programmable memory of claim 19, wherein each of the ~~circuit element~~ bipolar elements comprises a pnp device.

23. (Currently Amended) The programmable memory of claim [[19]] 22, further comprising a surrounding guard ring configured to isolate the ~~circuit element~~ pnp device from another ~~circuit element~~ pnp device.

24. (Currently Amended) The programmable memory of claim 23, wherein the surrounding guard ring comprises a p-type guard ring positioned around each ~~circuit element~~ pnp device.

25. (Original) The programmable memory of claim 23, wherein the surrounding guard ring comprises an n-type guard ring coupled to a high potential.

26. (Currently Amended) The programmable memory of claim 23, wherein each of the ~~fuse element~~ memory elements is positioned within the surrounding guard ring.

27. (Currently Amended) The programmable memory of claim 23, wherein each of the ~~fuse element~~ memory elements is positioned outside the surrounding guard ring.

28. (Currently Amended) The programmable memory of claim 22, wherein each pnp device has an n-type base, and wherein the ~~circuit elements~~ pnp devices on each row are joined at an n-type base

29. (Original) The programmable memory of claim 22, wherein the pnp devices on a row are isolated from the pnp devices of another row by a grounded p-type region.

30. (Original) The programmable memory of claim 22, and wherein the pnp devices on a row are isolated from the pnp devices of another row by a high potential n-type region.

31. (Currently Amended) The programmable memory of claim 19, wherein each of the ~~circuit element~~ bipolar elements comprises [[a]]an npn device.

32. (Currently Amended) The programmable memory of claim 19, wherein each of the ~~circuit element~~ bipolar elements further comprises a plurality of layered heaters.

33. (Currently Amended) The programmable memory of claim 19, further comprising a memory density ~~comprising~~ based on a sum of areas occupied by the memory ~~element~~ elements and [[a]] the plurality of programming ~~transistor~~ transistors, wherein the ~~fuse~~ memory density is at least 200 bits per square millimeter.

34. (Original) The programmable memory of claim 19, wherein the memory has at least 128 memory elements, and each memory element has a resistance of at least 5 ohms on the inkjet printhead chip.

35. (Currently Amended) A method of providing high fuse density in a printhead heater chip, the method comprising:

arranging a plurality of memory elements in a memory array;

programming the memory elements with a programming current with a plurality of field-effect programming transistors; and

isolating [[a]] the programming current in each of the memory ~~element~~ elements from another memory element in the memory array with a bipolar device.

36. (Currently Amended) The method of claim 35, wherein each of the memory ~~element~~ elements comprises a fuse element.

37. (Original) The method of claim 36, wherein the fuse element comprises at least one of tantalum aluminum, and tantalum aluminum nitride.

38. (Original) The method of claim 35, further comprising providing a plurality of layered heaters on the heater chip.

39. (Currently Amended) The method of claim 35, wherein at least one of the memory ~~element~~ elements comprises a floating gate element.

40. (Currently Amended) The method of claim 35, wherein each of the bipolar ~~device~~ devices comprises a pnp device.

41. (Original) The method of claim 40, further comprising isolating the pnp device with a surrounding guard ring.

42. (Currently Amended) The method of claim [[40]] 41, wherein the surrounding guard ring comprises a p-type guard ring, further comprising positioning the p-type guard ring around each pnp device.

43. (Currently Amended) The method of claim [[40]] 41, wherein the surrounding guard ring comprises an n-type guard ring, further comprising coupling the n-type guard ring to a high potential.

44. (Currently Amended) The method of claim [[40]] 41, further comprising positioning each of the memory ~~element~~ elements within the surrounding guard ring.

45. (Currently Amended) The method of claim [[40]] 41, further comprising positioning each of the memory ~~element~~ elements outside the surrounding guard ring.

46. (Original) The method of claim 40, wherein the memory array comprises rows and columns, and each pnp device has an n-type base, further comprising joining the pnp devices on each row at the n-type base.

47. (Original) The method of claim 40, further comprising:

arranging the pnp devices in a plurality of rows and columns intersecting each other; and

isolating the pnp devices on a row from the pnp devices of another row by a grounded p-type region.

48. (Original) The method of claim 40, further comprising:

arranging the pnp devices in a plurality of rows and columns intersecting each other; and

isolating the pnp devices on a row from the pnp devices of another row by a high potential n-type region.

49. (Currently Amended) The method of claim 35, wherein each of the bipolar ~~device~~ devices comprises [[a]]an npn device.

50. (Currently Amended) The method of claim 35, wherein each of the bipolar ~~device~~ devices comprises a diode.

51. (Currently Amended) The method of claim 35, further comprising providing a memory density of at least 200 bits per square millimeter including a sum of areas occupied by the memory ~~element~~ elements and [[a]] the plurality of programming ~~transistor~~ transistors.

52. (Currently Amended) The method of claim 35, further comprising providing at least 128 memory elements, [[and]] each of the memory ~~element~~ elements having a resistance of at least 5 ohms on the inkjet printhead chip.

53. (Currently Amended) A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having a plurality of memory elements, ~~and at least one~~ programming ~~transistor~~ transistors configured to program the memory elements with a programming current, and bipolar transistors, each of the bipolar transistors being associated with each of the memory elements, and configured to isolate the programming current in each of the memory elements from another memory element and having a memory density comprising a sum of areas occupied by the memory elements and the programming transistors ~~transistor~~, and wherein the memory density is at least 200 bits per square millimeter.

54. (Currently Amended) A programmable memory on an inkjet printhead chip, the memory comprising:

a memory array having ~~a plurality of~~ at least 128 memory elements; and

a plurality of field-effect programming transistors configured to program the memory elements with a programming current; and

a plurality of at least 128 bipolar devices, each of the at least 128 bipolar devices associated with each of the at least 128 memory elements, and configured to isolate the current in one memory element from another memory element, and wherein each memory element has a resistance of at least 5 ohms on the inkjet printhead chip.